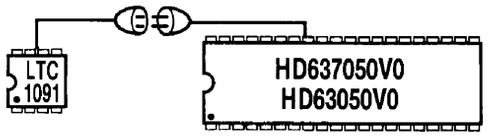
Interfacing the LTC1091 to the HD637050 MCU



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Introduction

This application note describes an interface between the LTC1091 10-bit data acquisition system and the Hitachi 63705 microcomputer. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data to the 63705 in 84μs. Configuration of the LTC1091 and the 63705 will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a half duplex synchronous format over D_{IN} and D_{OUT}.

The Hitachi Serial Communication Interface (SCI) is a synchronous, full duplex, serial port built into the 63705 that allows the user to construct a simple communication path to the LTC1091. SCI provides clock, transmit and receive lines that are compatible with the LTC1091. The only additional line required is one programmable output pin (C0) to control $\overline{CS}$ on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The 63705VOC was chosen for this application because it contains 4k bytes of EPROM which can be programmed by a 27256 EPROM programmer. The code shown will work on the 6305VO without modification.

The timing diagram of Figure 2 was obtained using an HP1631A logic analyzer. The 63705 clock was 4 MHz.

The analog section of the schematic of Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

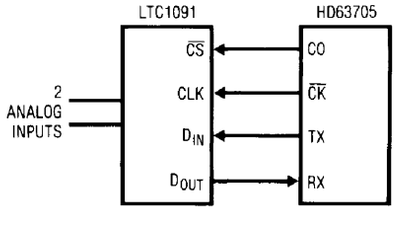

Figure 1. Schematic

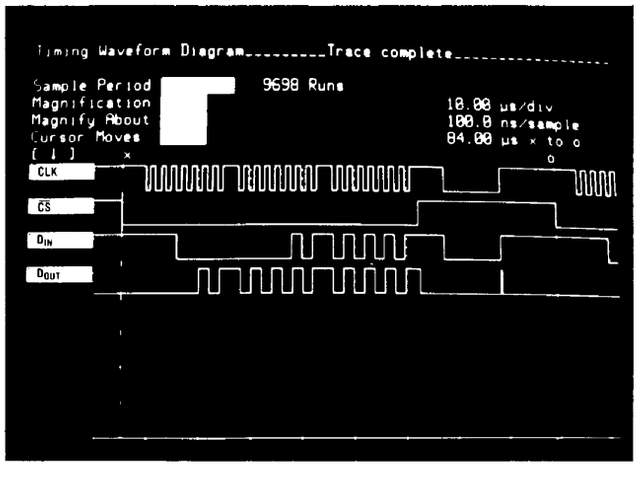

Figure 2. Timing Diagram

Software Description

The software configures and controls the SCI of the 63705. Additionally, the software manipulates C0 ($\overline{CS}$ of the LTC1091).

The code first configures the SCI control register (SCR). D3 and D4 are set as the SCI output and input respectively. D5 is selected as a clock output with a frequency one eighth the crystal frequency. Next, the SCI status register (SSR) is configured so that the interrupts are disabled. Data is transmitted on the falling edge of the clock and received on the rising edge of the clock.

Bit 0 of Port C is configured as an output by setting the first bit of the data direction register (address $06) to one. A D_{IN} word that configures the LTC1091 for CH1 with respect to ground and LSB first is stored in $50. Figure 3 shows how the D_{IN} word is composed. Note, that for LSB first format the D_{IN} word must be constructed opposite from MSB first format.

C0 is made to go low. D_{IN} for the LTC1091 is loaded into the SCI data register (SDR). Storing D_{IN} in the SDR causes the transfer to begin. When LSB first is selected, the LTC1091 first clocks out the data MSB first and then clocks out the data LSB first. After waiting for the first eight bits to be transferred the data containing the MSBs is loaded into the ACC. This starts the next transfer. The next eight bits are then shifted out and the first two LSBs from the LTC1091 are loaded into the accumulator and then stored in $61 of the 63705 RAM. The act of reading the

0	0	0	0	0 MSBF	1 O/S	1 S/D	1 START	$50

Figure 3. D_{IN} Word for LTC1091 Stored in 63705 RAM

LSB

LSB	1	0	X	X	X	X	X	X	$61

MSB

MSB	9	8	7	6	5	4	3	2	$62

D_{OUT} from LTC1091 stored in 63705 RAM

Figure 4. Memory Map

LABEL	MNEMONIC		COMMENTS
	LDA	#$E1	CONFIGURATION DATA FOR SCR
	STA	$10	LOAD DATA INTO SCR ($10)
	LDA	#$30	CONFIGURATION DATA FOR SSR
	STA	$11	LOAD DATA INTO SSR ($11)
	LDA	#$01	CONFIG. DATA FOR PORT C DDR
	STA	$06	LOAD DATA INTO PORT C DDR
	LDA	#$07	LOAD LTC1091 D_{IN} DATA INTO ACC
	STA	$50	LOAD LTC1091 D_{IN} DATA INTO $50
LOOP	LDA	$50	LOAD D_{IN} INTO ACC FROM $50
	BCLR	0,$02	C0 GOES LOW ($\overline{CS}$ GOES LOW)
	STA	$12	LOAD D_{IN} INTO SDR. START SCK
	BCLR	1,$06	FOR TIMING
	BCLR	1,$06	FOR TIMING
	BCLR	1,$06	FOR TIMING
	LDA	$12	LOAD DATA START NEXT CYCLE
	BCLR	1,$06	FOR TIMING
	BCLR	1,$06	FOR TIMING
	BCLR	1,$06	FOR TIMING
	LDA	$12	LOAD LSBs START NEXT CYCLE
	STA	$61	STORE LSBs IN $61
	BCLR	1,$06	FOR TIMING
	BCLR	1,$06	FOR TIMING
	BSET	0,$02	C0 GOES HIGH. ($\overline{CS}$ GOES HIGH)
	LDA	#$00	CONFIGURATION DATA FOR SCR
	STA	$10	DISABLE SCI
	LDA	$12	LOAD MSBs
	STA	$62	STORE MSBs IN $62
	LDA	#$E1	CONFIGURATION DATA FOR SCR
	STA	$10	TURN SCI ON

Figure 5. 63705 Code

LSBs into the ACC causes the next SCI transfer to begin. After the next eight bits are transferred, then C0 is set and the SCI port is disabled. The MSBs from the LTC1091 are loaded into the ACC and then stored in $62 of the 63705 RAM. The SCI port is then enabled. The data at this point is left justified as shown in Figure 4.

Summary

A four wire interface between the LTC1091 and the Hitachi 63705 with a combined data conversion and transfer time of 84μs was demonstrated. The interface used the serial (SCI) port of the 63705. Because the SCI port transfers data LSB first, care must be taken to properly construct the D_{IN} word so that the bits are transmitted in the proper order to the LTC1091. The 10 data bits of the LTC1091 are shifted MSB first and then LSB first in three eight bit transfers. The data is stored left justified in the 63705's internal RAM.